REMARKS/ARGUMENTS

In view of the foregoing proposed amendments and the following remarks, reconsideration of this application is requested. Claims 7-28 are now pending with claims 7, 11, 18, and 22 being independent. Claims 1-6 have been canceled. No new matter has been introduced.

Applicants have proposed an amendment to the specification on page 11, line 4 to correct a typographical error. Finally, Applicants have checked the specification for minor errors.

Claim 7, if amended as proposed, describes a method, comprising fetching and decoding instructions in a first processor, detecting an unsupported instruction that is not executable by the first processor, executing said unsupported instruction in a second processor, and providing the first processor with a supported instruction that is executable in the first processor by loading the supported instruction in decode logic of the first processor without the first processor fetching **any portion of** said **supported** instruction.

Claim 11, if amended as proposed, describes a system, comprising a first processor having fetch logic and decode logic, the first processor fetches supported instructions from memory using said fetch logic and decodes said supported instructions with said decode logic, a second processor, the second processor executes unsupported instructions, means for loading a supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch **any portion of** the supported instruction, means for coordinating when said loading the supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch **any portion of** the supported instruction occurs.

Independent claims 7, 11, 18, and 22 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Park et al. (U.S. Patent No. 6,832,305). Applicants request reconsideration and withdrawal of this rejection for at least the reason that Park does not describe or suggest the recitation in claims 7 and 18, if amended as proposed, of providing the first processor with a supported instruction that is executable in the first processor by loading the supported instruction in decode logic of the first processor **without the first processor fetching *any portion of* said *supported* instruction**. Park does not describe or suggest the recitation in claims 11 and 22, if amended as proposed, of means for loading a supported instruction in said decode logic of the

first processor so that the first processor decodes **but does not fetch *any portion of* the *supported* instruction**.

Park in col. 4, lines 31-48, referring to Figure 1, describes that the 16 'm' bit instruction fetched from MPM 140 is sent to CPU 110, first into fetch buffer 111. At the output of fetch buffer 111, the 3 'c' MSB bits are branched off the predecoder 113, where if the 'c' bits signal a coprocessor operation, signal COPI 116 and CCLK 119 are activated. Thirteen of the 16 m bits (m-c) are branched to coprocessor 120. CCLK 119 clocks into the coprocessor instruction register 121 the entire 29 bits of coprocessor instruction, with 13 bits from the output of CPU instruction fetch buffer 111 and 16 'n' bits from CPM 160 through **coprocessor instruction fetch buffer 126**. Thus, the **coprocessor fetches** 'n' bits of the ***supported* instruction** to form a 13+n bit coprocessor instruction that is decoded and executed by the coprocessor. Figure 1 shows Coprocessor Instruction **Fetch** Buffer 126 for **fetching *part* of the coprocessor instruction**. Indeed, the Examiner agrees with the Applicants that Park has **part** of the coprocessor instruction being fetched by the coprocessor with the remainder coming from the processor. *Final Office Action* mailed March 8, 2007, paragraph 37, page 11. Therefore, Park does not describe or suggest the recitation in claims 7 and 18, if amended as proposed, of providing the first processor with a supported instruction that is executable in the first processor by loading the supported instruction in decode logic of the first processor **without the first processor fetching *any portion of* said *supported* instruction**. Park also does not describe or suggest the recitation in claims 11 and 22, if amended as proposed, of means for loading a supported instruction in said decode logic of the first processor so that the first processor decodes **but does not fetch *any portion of* the *supported* instruction**.

For at least the reasons given above, Applicants respectfully submit that claims 7, 11, 18, and 22, if amended as proposed, are patentable over Park.

Claims 8-10 depend from independent claim 7, claims 12 and 14-16 depend from independent claim 11, claims 19-21 depend from claim 18, and claims 23 and 25-27 depend from claim 22. Accordingly, Applicants request reconsideration and withdrawal of the rejections for claims 8-10, 12, 14-16, 19-21, 23, and 25-27 for the reasons discussed above with respect to claims 7, 11, 18, and 22, if amended as proposed.

Dependent claims 17 and 28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. Patent No. 6,832,305). Park does not describe or suggest all of the limitations of claims 11 and 22, if amended as proposed, as described above. Because claim 17 depends from claim 11, and claim 28 depends from claim 22, Applicants request reconsideration and withdrawal of the rejections for claims 17 and 28 for the reasons discussed above with respect to claims 11 and 22, if amended as proposed.

Claims 13 and 24 stand rejected under 35 U.S.C. § 103(a) as obvious over Park in view of Chaudhry et al., U.S. Pat. No. 6,681,318 ("Chaudhry"). Applicants respectfully submit that neither Park nor Chaudhry, whether considered singly or in combination, teach or suggest all of the limitations in claims 13 and 24. Applicants offer the following comments in support of their position.

Establishing a case of prima facie obviousness requires that all of the claim limitations must be suggested or taught in the prior art references. *In re Royka*, 180 U.S.P.Q. 580 (C.C.P.A. 1974). For at least the reasons set forth above in Applicants remarks concerning the rejection of claims 11 and claim 22 under 35 U.S.C. § 102(e) as being anticipated by Park, Applicants submit that neither Park nor Chaudhry whether considered singly or in combination, teach or suggest all of the limitations of claims 11 and 22, if amended as proposed, from which claims 13 and 24 depend, respectively. In particular, none of the cited references whether considered singly or in combination, teach or suggest "means for ***loading*** **a supported instruction** ***in said decode logic*** **of the** ***first*** **processor** so that the ***first*** **processor** ***decodes*** but does not fetch **any portion of** the **supported** instruction" as recited in claims 11 and 22, if amended as proposed (emphasis added). Consequently, the cited references cannot teach all of the limitations of claims 13 and 24.

In view of these remarks and proposed amendments, Applicants submit that this application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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